

<b>INFORMATION DISCLOSURE STATEMENT</b>		Atty Docket: 02GR119554482 Serial No.: Not Yet Assigned Applicant: Joet et al. Filing Date: Herewith Group: 2816		10/688, 208		
<b>U.S. PATENT DOCUMENTS</b>						
Examiner Initials	Document Number	Date	Name	Class	Sub Class	Filing Date
M	AA	5,821,816	Patterson	331	1A	✓
M	AB	<del>2002/0140542</del>	Stockton	331	11	4/3/01
	AC	6509,800	X			
	AD					
	AE					
	AF					
	AG					
	AH					
<b>FOREIGN PATENT DOCUMENTS</b>						
Document Number	Date	Country	Class	Sub Class	Translation	
AI		X				
AJ						
AK						
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)</b>						
M	AL	Djemouai et al., New Frequency-Locked Loop Based on CMOS Frequency-to-Voltage Converter: Design and Implementation, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 48, No. 5, May 2001, Pages 441-449, XP002247796				
	AM	X				
	AN					
	AO					
	AP					
EXAMINER: <i>Nov</i>			DATE CONSIDERED: 10/22/09			

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.